DATA SHEET

DDR SDRAM

184Pin Unbuffered DIMM

Based on Micron 256Mb M-die

66-pin TSOP With Lead-Free

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Revision History

Revision No.	History	Draft Date	Remark
1.0	Initial Release	December, 2013	

Features

- Package: 184-pin dual-in-line DDR memory module (UDIMM)
- Dansity: 512MB
- Organization: 64Mb*72,2 Rank
- Power supply: VDD = 2.5 V ±0.2V
- Data rates: 333Mbps(max.)
- 8 independent internal banks
- Bi-directional Differential data strobe (DQS, DQS#)
- Differential clock inputs (CK,CK#)
- Commands entered on each positive CK edge
- Two-bit pre-fetch architecture
- DQS edge-aligned with data for READs
- DQS center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Data mask (DM) for masking write data
- Burst lengths(BL): 2,4 or 8
- Serial Presence Detect (SPD) with EEPROM
- Operating case temperature range: Tc = 0℃ ~ 75℃
- Auto refresh and self refresh modes: 7.8125㎲ maximum average periodic refresh interval
- Lead-free
- For contact pads, electrolytic gold plating

Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Gold plating thickness(min.)
RME1391MM28C6T-333A	512MB	64M*72	32Mx8(MT46V32M8P-5B:M) *18	2	0.76um

Detailed Information

For detailed electrical specifications and further information, please refer to the component DDR SDRAM datasheet MT46V32M8P-5B:M.

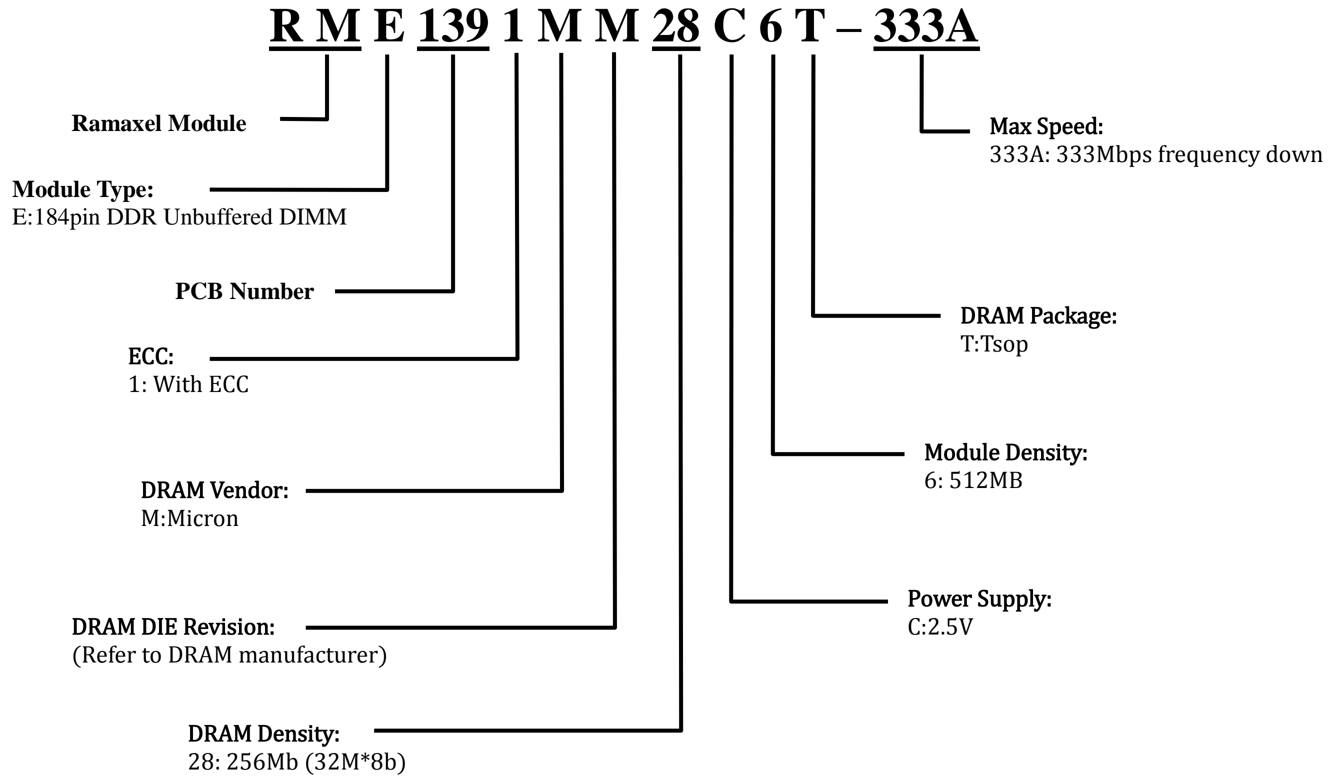
Key Parameters

Speed Grade	Clock Rate(MHz)			Data-Out Window	Access Window	DQS-DQ Skew
	CL=2	CL=2.5	CL=3			
DDR333	133	167	n/a	2.0ns	±0.70ns	0.45ns

Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
32M*8(256Mb) based module	A0-A12	A0-A9	BA0-BA1	A10/AP

Part Number



Pin Assignments

Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)			Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)		
Pin #	x64 Nonparity	x72 ECC	Pin #	x64 Nonparity	x72 ECC	Pin #	x64 Nonparity	x72 ECC	Pin #	x64 Nonparity	x72 ECC
1	VREF	VREF	93	VSS	VSS	48	A0	A0	140	NC	DM8, DQS17
2	DQ0	DQ0	94	DQ4	DQ4	49	NC	CB2	141	A10/AP	A10/AP
3	VSS	VSS	95	DQ5	DQ5	50	VSS	VSS	142	NC	CB6
4	DQ1	DQ1	96	VDDQ	VDDQ	51	NC	CB3	143	VDDQ	VDDQ
5	DQS0	DQS0	97	DM0, DQS9	DM0, DQS9	52	BA1	BA1	144	NC	CB7
6	DQ2	DQ2	98	DQ6	DQ6	KEY			KEY		
7	VDD	VDD	99	DQ7	DQ7	53	DQ32	DQ32	145	VSS	VSS
8	DQ3	DQ3	100	VSS	VSS	54	VDDQ	VDDQ	146	DQ36	DQ36
9	NC	NC	101	NC	NC	55	DQ33	DQ33	147	DQ37	DQ37
10	NC	NC	102	NC, TEST	NC, TEST	56	DQS4	DQS4	148	VDD	VDD
11	VSS	VSS	103	NC (FETEN)	NC (FENTEN)	57	DQ34	DQ34	149	DM4, DQS13	DM4, DQS13
12	DQ8	DQ8	104	VDDQ	VDDQ	58	VSS	VSS	150	DQ38	DQ38
13	DQ9	DQ9	105	DQ12	DQ12	59	BA0	BA0	151	DQ39	DQ39
14	DQS1	DQS1	106	DQ13	DQ13	60	DQ35	DQ35	152	VSS	VSS
15	VDDQ	VDDQ	107	DM1, DQS10	DM1, DQS10	61	DQ40	DQ40	153	DQ44	DQ44
16	CK1	CK1	108	VDD	VDD	62	VDDQ	VDDQ	154	/RAS	/RAS
17	/CK1	/CK1	109	DQ14	DQ14	63	/WE	/WE	155	DQ45	DQ45
18	VSS	VSS	110	DQ15	DQ15	64	DQ41	DQ41	156	VDDQ	VDDQ
19	DQ10	DQ10	111	CKE1	CKE1	65	/CAS	/CAS	157	/S0	/S0
20	DQ11	DQ11	112	VDDQ	VDDQ	66	VSS	VSS	158	/S1	/S1
21	CKE0	CKE0	113	BA2	BA2	67	DQS5	DQS5	159	DM5, DQS14	DM5, DQS14
22	VDDQ	VDDQ	114	DQ20	DQ20	68	DQ42	DQ42	160	VSS	VSS
23	DQ16	DQ16	115	A12	A12	69	DQ43	DQ43	161	DQ46	DQ46
24	DQ17	DQ17	116	VSS	VSS	70	VDD	VDD	162	DQ47	DQ47
25	DQS2	DQS2	117	DQ21	DQ21	71	NC, /S2	NC, /S2	163	NC, /S3	NC, /S3
26	VSS	VSS	118	A11	A11	72	DQ48	DQ48	164	VDDQ	VDDQ
27	A9	A9	119	DM2, DQS11	DM2, DQS11	73	DQ49	DQ49	165	DQ52	DQ52
28	DQ18	DQ18	120	VDD	VDD	74	VSS	VSS	166	DQ53	DQ53
29	A7	A7	121	DQ22	DQ22	75	/CK2	/CK2	167	A13	A13
30	VDDQ	VDDQ	122	A8	A8	76	CK2	CK2	168	VDD	VDD
31	DQ19	DQ19	123	DQ23	DQ23	77	VDDQ	VDDQ	169	DM6, DQS15	DM6, DQS15
32	A5	A5	124	VSS	VSS	78	DQS6	DQS6	170	DQ54	DQ54
33	DQ24	DQ24	125	A6	A6	79	DQ50	DQ50	171	DQ55	DQ55
34	VSS	VSS	126	DQ28	DQ28	80	DQ51	DQ51	172	VDDQ	VDDQ
35	DQ25	DQ25	127	DQ29	DQ29	81	VSS	VSS	173	NC	NC
36	DQS3	DQS3	128	VDDQ	VDDQ	82	VDDID	VDDID	174	DQ60	DQ60
37	A4	A4	129	DM3, DQS12	DM3, DQS12	83	DQ56	DQ56	175	DQ61	DQ61
38	VDD	VDD	130	A3	A3	84	DQ57	DQ57	176	VSS	VSS
39	DQ26	DQ26	131	DQ30	DQ30	85	VDD	VDD	177	DM7, DQS16	DM7, DQS16
40	DQ27	DQ27	132	VSS	VSS	86	DQS7	DQS7	178	DQ62	DQ62
41	A2	A2	133	DQ31	DQ31	87	DQ58	DQ58	179	DQ63	DQ63
42	VSS	VSS	134	NC	CB4	88	DQ59	DQ59	180	VDDQ	VDDQ
43	A1	A1	135	NC	CB5	89	VSS	VSS	181	SA0	SA0
44	NC	CB0	136	VDDQ	VDDQ	90	NC	NC	182	SA1	SA1
45	NC	CB1	137	CK0	CK0	91	SDA	SDA	183	SA2	SA2
46	VDD	VDD	138	/CK0	/CK0	92	SCL	SCL	184	VDDSPD	VDDSPD
47	NC	DQS8	139	VSS	VSS						

NC = No Connect NU = Not Useable

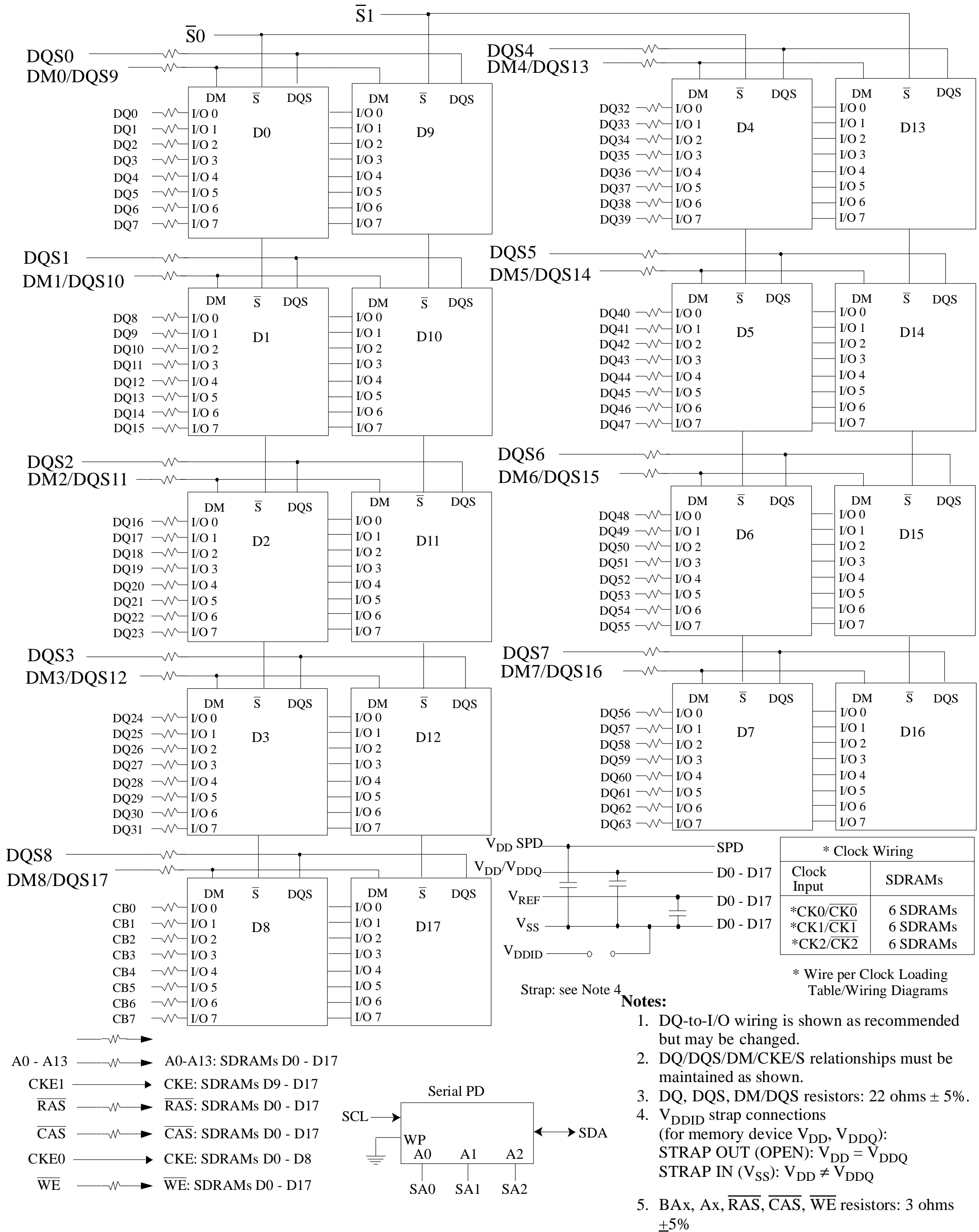
Note: The TEST pin is reserved for bus analysis probes and is not connected on normal memory module (DIMMs)

Pin Functional Description

Symbol	Type	Polarity	Function
CK0 - CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs. All the DDR SDRAM addr/cntl inputs are sampled on the rising edge of their associated clocks.
$\overline{CK}0$ - $\overline{CK}2$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S}0$, $\overline{S}1$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL2 inputs.
V_{DDQ}	Supply		Power supply for the DDR SDRAM output buffers to provide improved noise immunity. For all current DDR unbuffered DIMM designs, V_{DDQ} shares the same power plane as V_{DD} pins.
BA0,1	(SSTL)	—	Selects which SDRAM bank of four is activated.
A0 - A9 A10/AP, A11-A13	(SSTL)	—	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-12 defines the column address (CA0-CA12) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	(SSTL)	—	Data and Check Bit Input/Output pins.
DM0-DM8	(SSTL)	Active High	Masks write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the write command is registered into the SDRAM.
V_{DD}, VSS	Supply		Power and ground for the DDR SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to a single combined V_{DD}/V_{DDQ} plane on these modules.
DQS0-DQS8	(SSTL)	Negative and Positive Edge	Data strobe for input and output data. For the x16, LDQS corresponds to the data on DQ0-7, UDQS corresponds to the data on DQ8-15.
SA0 - 2		—	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup.
V_{DD} SPD	Supply		Power supply for SPD EEPROM. This supply is separate from the V_{DD}/V_{DDQ} power plane. EEPROM supply is operable from 2.3 V to 3.6 V.

Block Diagram

Raw Card B (x72 DIMM, populated as two physical ranks of x8 DDR SDRAMs)



* Clock Wiring	
Clock Input	SDRAMs
*CK0/$\overline{CK0}$	6 SDRAMs
*CK1/$\overline{CK1}$	6 SDRAMs
*CK2/$\overline{CK2}$	6 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$
5. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: 3 ohms ±5%

Electrical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units
V_{DD} supply voltage relative to V_{SS}	–1V	3.6V	V
V_{DDQ} supply voltage relative to V_{SS}	–1V	3.6V	V
V_{REF} and inputs voltage relative to V_{SS}	–1V	3.6V	V
I/O pins voltage relative to V_{SS}	–0.5V	V_{DDQ} + 0.5V	V
Storage temperature (plastic)	–55	150	°C
Short circuit output current	–	50	mA

DC Electrical Characteristics and Operating

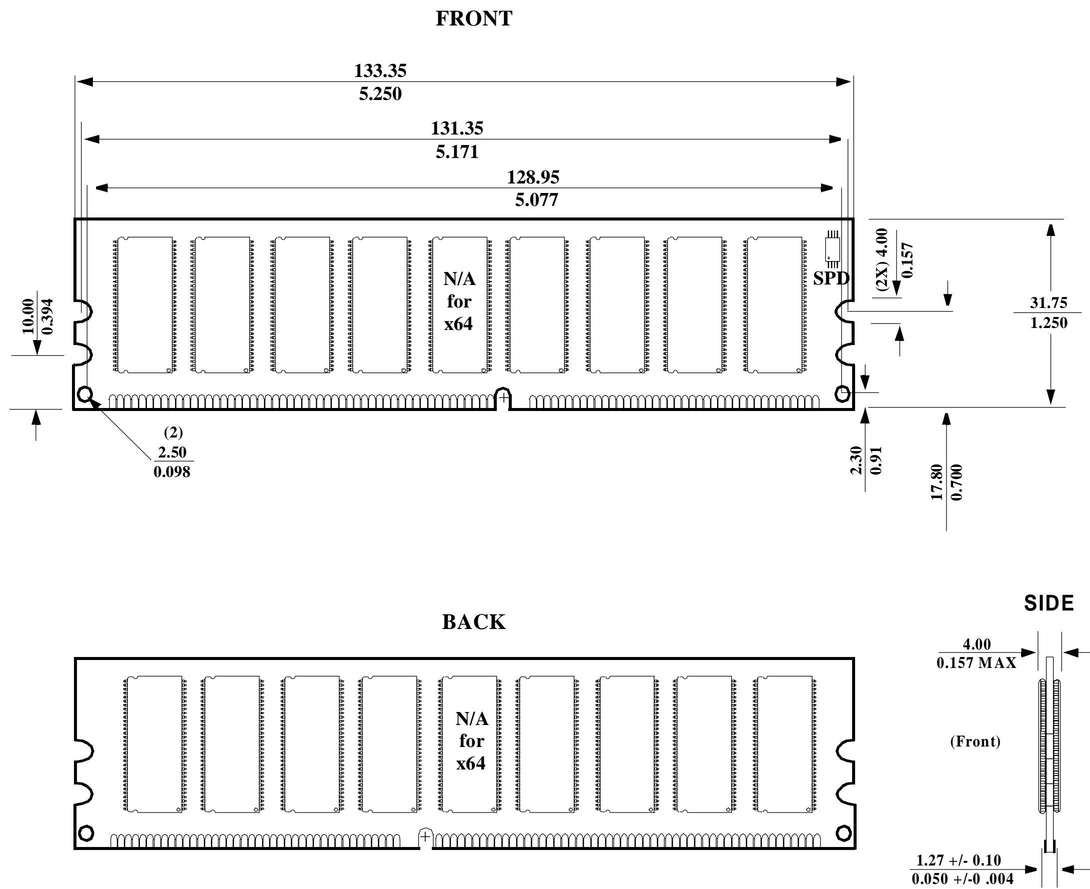
Parameter/Condition		Symbol	Min	Max	Units	Notes
Supply voltage		V_{DD}	2.3	2.7	V	37, 42
I/O supply voltage		V_{DDQ}	2.3	2.7	V	37, 42, 45
I/O reference voltage		V_{REF}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	7, 45
I/O termination voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	8, 45
Input high (logic 1) voltage		$V_{IH(DC)}$	V_{REF} + 0.15	V_{DD} + 0.3	V	29
Input low (logic 0) voltage		$V_{IL(DC)}$	–0.3	V_{REF} - 0.15	V	29
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)		I_I	–2	2	µA	
Output leakage current: (DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})		I_{OZ}	–5	5	µA	
Full-drive option output levels (x4, x8, x16):	High current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OH}	–16.8	–	mA	38, 40
	Low current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OL}	16.8	–	mA	
Reduced-drive option output levels:	High current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OHR}	–9	–	mA	39, 40
	Low current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OLR}	9	–	mA	
Ambient operating temperatures	Commercial	T_A	0	70	°C	
	Industrial	T_A	–40	85	°C	

IDD Specifications and Conditions

DC Characteristics 1 (VDD = 2.5 V ±0.2V, VSS = 0V)

Data rate (Mbps)			333		
Parameter		**Symbol**	**max.**	**Unit**	**Notes**
Operating one bank active-precharge current		IDD0	1170	mA	
Operating one bank active-read-precharge current		IDD1	1440	mA	
Precharge power-down current		IDD2P	45	mA	
Idle standby current		IDD2F	405	mA	
Active power-down standby current		IDD3P	315	mA	
Active standby current		IDD3N	450	mA	
Operating burst read current		IDD4R	1485	mA	
Operating burst write current		IDD4W	1575	mA	
Auto refresh current	tRFC= tRFC(MIN)	IDD5	2610	mA	
	tRFC= 7.8125us	IDD5A	90	mA	
Self refresh current		IDD6	45	mA	
Operating bank interleave read current		IDD7	3645	mA	

Dimensions



Note: All dimensions are typical unless otherwise stated $\frac{\text{millimeters}}{\text{inches}}$

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stresson these components to prevent damaging them.In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

NOTES FOR CMOS DEVICES

1) PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

2) HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.