

DATA SHEET

DDR2 SDRAM

240Pin Unbuffered DIMM

Based on Micron 1Gb H-die

60-ball FBGA With Lead-Free
(RoHS compliant)

Revision History

Revision No.	History	Draft Date	Remark
1.0	Initial Release	December, 2013	

Features

- Package: 240-pin dual-in-line DDR2 memory module (UDIMM)
- Density: 2GB
- Organization: 256Mb*72, 2 Rank
- Power supply: VDD = 1.8 V ±0.1V
- Data rates: 667Mbps(max.)
Backward compatible to 533Mbps/400Mbps
- 8 independent internal banks
- Bi-directional Differential data strobe (DQS, DQS#)
- Differential clock inputs (CK,CK#)
- Commands entered on each rising CK edge
- Four-bit pre-fetch architecture
- DQS edge-aligned with data for READs
- DQS center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Data mask (DM) for masking write data
- Burst lengths(BL): 4 or 8
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Operating case temperature range:
Tc = 0°C ~ 95°C
- Average refresh period:
7.8us at 0 ~ 85°C; 3.9us at 85 ~ 95°C
- Lead-free (RoHS compliant)
- For contact pads, electrolytic gold plating

Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Gold plating thickness(min.)
RML1531MH48D8F-667A	2GB	256M*72	128Mx8(MT47H128M8CF-25:H) *18	2	0.76um

Detailed Information

For detailed electrical specifications and further information, please refer to the component DDR2 SDRAM datasheet MT47H128M8CF-25:H.

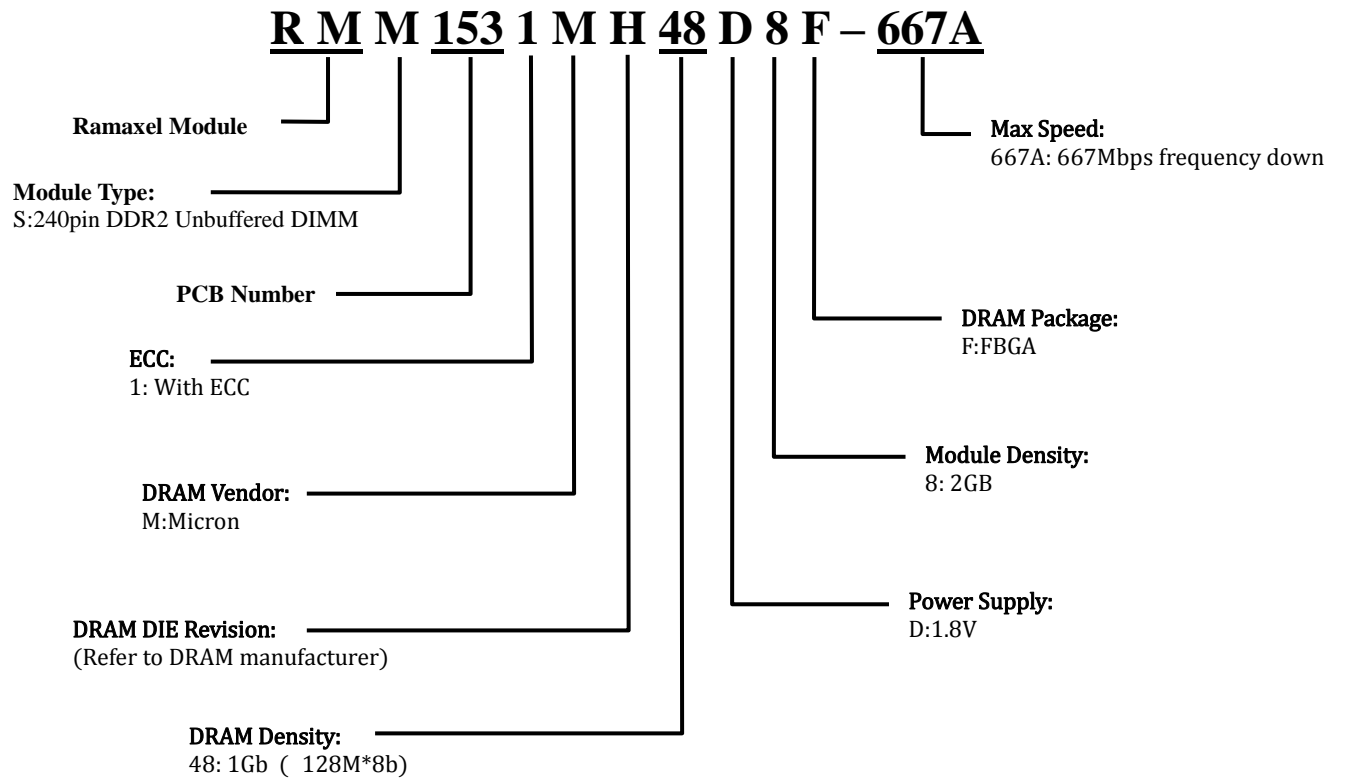
Key Parameters

Speed	DDR2-400	DDR2-533	DDR2-667	Unit
	3-3-3	4-4-4	5-5-5	
tCK(min)	5	3.75	3	ns
CAS Latency	3	3,4	3,4,5	tCK
tRCD(min)	15	15	15	ns
tRP(min)	15	15	15	ns
tRAS(min)	40	45	45	ns
tRC(min)	55	60	60	ns

Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
128*8(2Gb) based module	A0-A13	A0-A9	BA0-BA2	A10/AP

Part Number



Pin Assignments

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V _{REF}	121	V _{SS}	31	DQ19	151	V _{SS}	61	A4	181	V _{DDQ}	91	V _{SS}	211	DM5/DQS14
2	V _{SS}	122	DQ4	32	V _{SS}	152	DQ28	62	V _{DDQ}	182	A3	92	$\overline{\text{DQS}}_5$	212	NC, $\overline{\text{DQS}}_4$
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V _{SS}
4	DQ1	124	V _{SS}	34	DQ25	154	V _{SS}	64	V _{DD}	184	V _{DD}	94	V _{SS}	214	DQ46
5	V _{SS}	125	DM0/DQS9	35	V _{SS}	155	DM3/DQS12	KEY				95	DQ42	215	DQ47
6	$\overline{\text{DQS}}_0$	126	NC, $\overline{\text{DQS}}_9$	36	$\overline{\text{DQS}}_3$	156	NC, $\overline{\text{DQS}}_12$	65	V _{SS}	185	CK0	96	DQ43	216	V _{SS}
7	DQS0	127	V _{SS}	37	DQS3	157	V _{SS}	66	V _{SS}	186	$\overline{\text{CK}}_0$	97	V _{SS}	217	DQ52
8	V _{SS}	128	DQ6	38	V _{SS}	158	DQ30	67	V _{DD}	187	V _{DD}	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC, Par_In	188	A0	99	DQ49	219	V _{SS}
10	DQ3	130	V _{SS}	40	DQ27	160	V _{SS}	69	V _{DD}	189	V _{DD}	100	V _{SS}	220	RFU, $\overline{\text{S}}_2$
11	V _{SS}	131	DQ12	41	V _{SS}	161	CB4	70	A10/ AP	190	BA1	101	SA2	221	RFU, $\overline{\text{S}}_3$
12	DQ8	132	DQ13	42	CB0	162	CB5	71	BA0	191	V _{DDQ}	102	NC(TEST)	222	V _{SS}
13	DQ9	133	V _{SS}	43	CB1	163	V _{SS}	72	V _{DDQ}	192	$\overline{\text{RAS}}$	103	V _{SS}	223	DM6/DQS15
14	V _{SS}	134	DM1/DQS10	44	V _{SS}	164	DM8/DQS17	73	$\overline{\text{WE}}$	193	$\overline{\text{S}}_0$	104	$\overline{\text{DQS}}_6$	224	NC, $\overline{\text{DQS}}_15$
15	$\overline{\text{DQS}}_1$	135	NC, $\overline{\text{DQS}}_{10}$	45	$\overline{\text{DQS}}_8$	165	NC, $\overline{\text{DQS}}_{17}$	74	$\overline{\text{CAS}}$	194	V _{DDQ}	105	DQS6	225	V _{SS}
16	DQS1	136	V _{SS}	46	DQS8	166	V _{SS}	75	V _{DDQ}	195	ODT0	106	V _{SS}	226	DQ54
17	V _{SS}	137	RFU	47	V _{SS}	167	CB6	76	NC, $\overline{\text{S}}_1$	196	A13, NC	107	DQ50	227	DQ55
18	$\overline{\text{RESET}}$	138	RFU	48	CB2	168	CB7	77	NC, ODT1	197	V _{DD}	108	DQ51	228	V _{SS}
19	NC	139	V _{SS}	49	CB3	169	V _{SS}	78	V _{DDQ}	198	V _{SS}	109	V _{SS}	229	DQ60
20	V _{SS}	140	DQ14	50	V _{SS}	170	V _{DDQ}	79	V _{SS}	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V _{DDQ}	171	NC, CK1	80	DQ32	200	DQ37	111	DQ57	231	V _{SS}
22	DQ11	142	V _{SS}	52	CKE0	172	V _{DD}	81	DQ33	201	V _{SS}	112	V _{SS}	232	DM7/DQS16
23	V _{SS}	143	DQ20	53	V _{DD}	173	A15, NC	82	V _{SS}	202	DM4/DQS13	113	$\overline{\text{DQS}}_7$	233	NC, $\overline{\text{DQS}}_{16}$
24	DQ16	144	DQ21	54	BA2, NC	174	A14, NC	83	$\overline{\text{DQS}}_4$	203	NC, $\overline{\text{DQS}}_{13}$	114	DQS7	234	V _{SS}
25	DQ17	145	V _{SS}	55	$\overline{\text{NC, Err_Out}}$	175	V _{DDQ}	84	DQS4	204	V _{SS}	115	V _{SS}	235	DQ62
26	V _{SS}	146	DM2/DQS11	56	V _{DDQ}	176	A12	85	V _{SS}	205	DQ38	116	DQ58	236	DQ63
27	$\overline{\text{DQS}}_2$	147	NC, $\overline{\text{DQS}}_{11}$	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V _{SS}
28	DQS2	148	V _{SS}	58	A7	178	V _{DD}	87	DQ35	207	V _{SS}	118	V _{SS}	238	VDDSPD
29	V _{SS}	149	DQ22	59	V _{DD}	179	A8	88	V _{SS}	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V _{SS}				

NC = No Connect; NU = Not Useable, RFU = Reserved Future Use.

1. CK1, CK1, CK2, CK2 (pins 137, 138, 220, 221) are for Unbuffered DIMM clock.

Pins 137, 138 are RFU on registered DIMMs; pins 220, 221 are used for 4 rank RDIMMs.

2. RESET (pin 18) is connected to both OE of the PLL and Reset of the register.

3. The TEST pin (pin 102) is reserved for bus analysis probes and is not connected on normal modules (DIMMs).

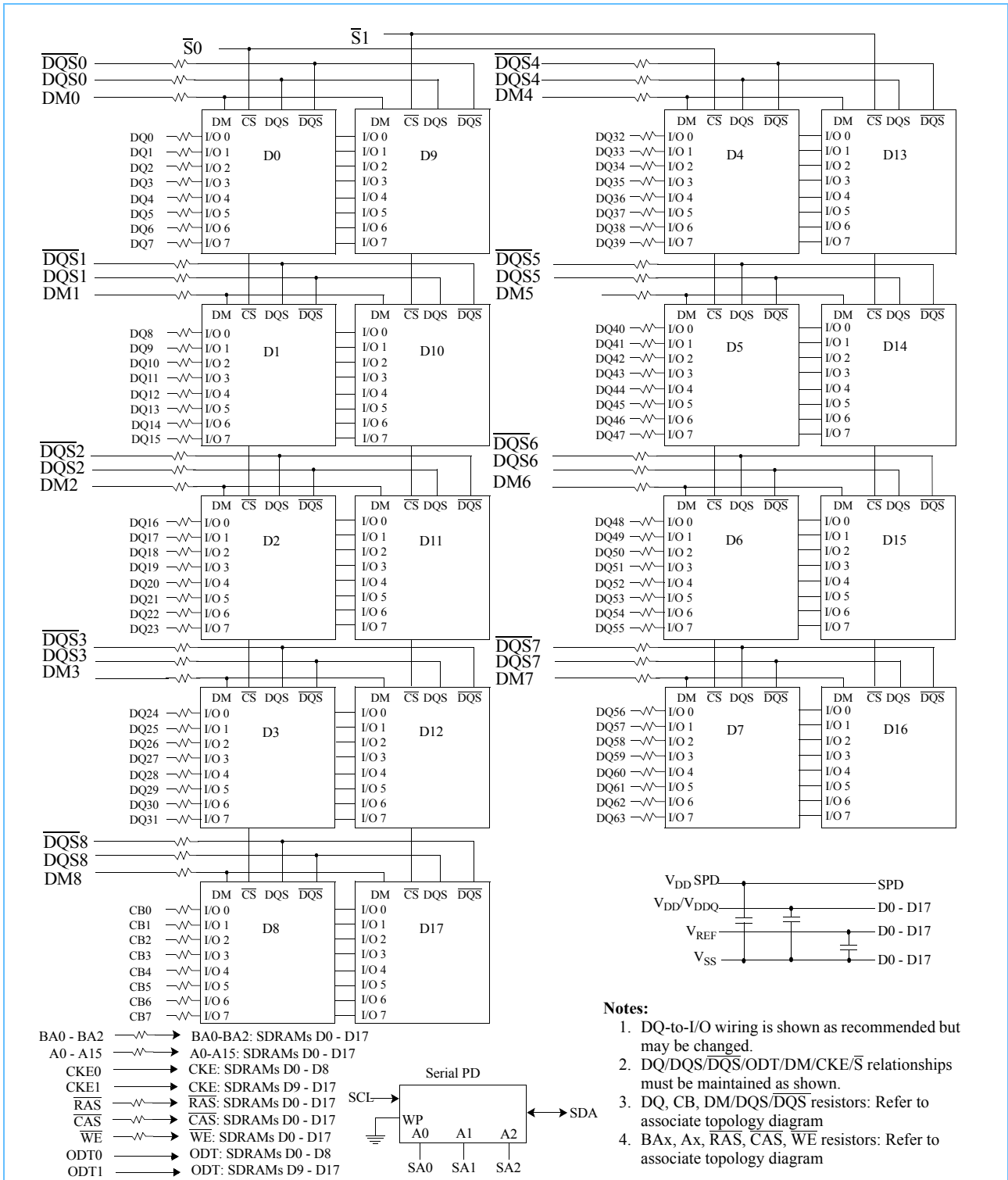
4. NC/Err_Out (pin 55) and NC/Par_In (pin 68) are optional function to check address and command parity.

Pin Functional Description

Symbol	Type	Polarity	Function
CK0	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
$\overline{\text{CK0}}$	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
$\overline{\text{S}}[3:0]$	IN	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both $\overline{\text{S}}[0:1]$ are high, all register outputs (except CKE, ODT and Chip select) remain in the previous state. For modules supporting 4 ranks, $\overline{\text{S}}[2:3]$ operate similarly to $\overline{\text{S}}[0:1]$ for a second set of register outputs.
ODT[1:0]	IN	Active High	On-Die Termination control signals
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	IN	Active Low	When sampled at the positive rising edge of the clock, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR2 SDRAM output buffers to provide improved noise immunity
BA[2:0]	IN	—	Selects which SDRAM bank of four or eight is activated.
A[15:11, 10/AP,9:0]	IN	—	During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1,BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1 or BA2. If AP is low, BA0 and BA1 and BA2 are used to define which bank to precharge.
DQ[63:0], CB[7:0]	I/O	—	Data and Check Bit Input/Output pins
DM[8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
V_{DD} , V_{SS}	Supply		Power and ground for the DDR2 SDRAM input buffers and core logic.
DQS[17:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
$\overline{\text{DQS}}[17:0]$	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
SA[2:0]	IN	—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pullup.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus line to V_{DDSPD} on the system planar to act as a pullup.
V_{DDSPD}	Supply		Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports from 1.7 Volt to 3.6 Volt (nominal 1.8 Volt, 2.5 Volt and 3.3 Volt) operation.
$\overline{\text{RESET}}$	IN		The $\overline{\text{RESET}}$ pin is connected to the $\overline{\text{RST}}$ pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (the PLL will remain synchronized with the input clock)
Par_In	IN		Parity bit for the Address and Control bus. ("1 ": Odd, "0 ": Even)
$\overline{\text{Err_Out}}$	OUT		Parity error found in the Address and Control bus
TEST			Used by memory bus analysis tools (unused on memory DIMMs)

Block Diagram

Raw Card G (x72 DIMM, populated as two physical ranks of x8 DDR2 SDRAMs)



Electrical Specifications

All voltages are referenced to VSS (GND).

Absolute Maximum DC Rating

Parameter	Symbol	Min	Max	Units	Notes
V _{DD} supply voltage relative to V _{SS}	V _{DD}	-1.0	2.3	V	1
V _{DDQ} supply voltage relative to V _{SSQ}	V _{DDQ}	-0.5	2.3	V	1, 2
V _{DDL} supply voltage relative to V _{SSL}	V _{DDL}	-0.5	2.3	V	1
Voltage on any ball relative to V _{SS}	V _{IN} , V _{OUT}	-0.5	2.3	V	3
Input leakage current; any input 0V ≤ V _{IN} ≤ V _{DD} ; all other balls not under test = 0V	I _I	-5	5	μA	
Output leakage current; 0V ≤ V _{OUT} ≤ V _{DDQ} ; DQ and ODT disabled	I _{OZ}	-5	5	μA	
V _{REF} leakage current; V _{REF} = Valid V _{REF} level	I _{VREF}	-2	2	μA	

- Notes:
1. V_{DD}, V_{DDQ}, and V_{DDL} must be within 300mV of each other at all times; this is not required when power is ramping down.
 2. V_{REF} ≤ 0.6 × V_{DDQ}; however, V_{REF} may be ≥ V_{DDQ} provided that V_{REF} ≤ 300mV.
 3. Voltage on any I/O may not exceed voltage on V_{DDQ}.

Temperature Limits

Parameter	Symbol	Min	Max	Units	Notes
Storage temperature	T _{STG}	-55	150	°C	1
Operating temperature: commercial	T _C	0	85	°C	2, 3
Operating temperature: industrial	T _C	-40	95	°C	2, 3, 4
	T _A	-40	85	°C	4, 5

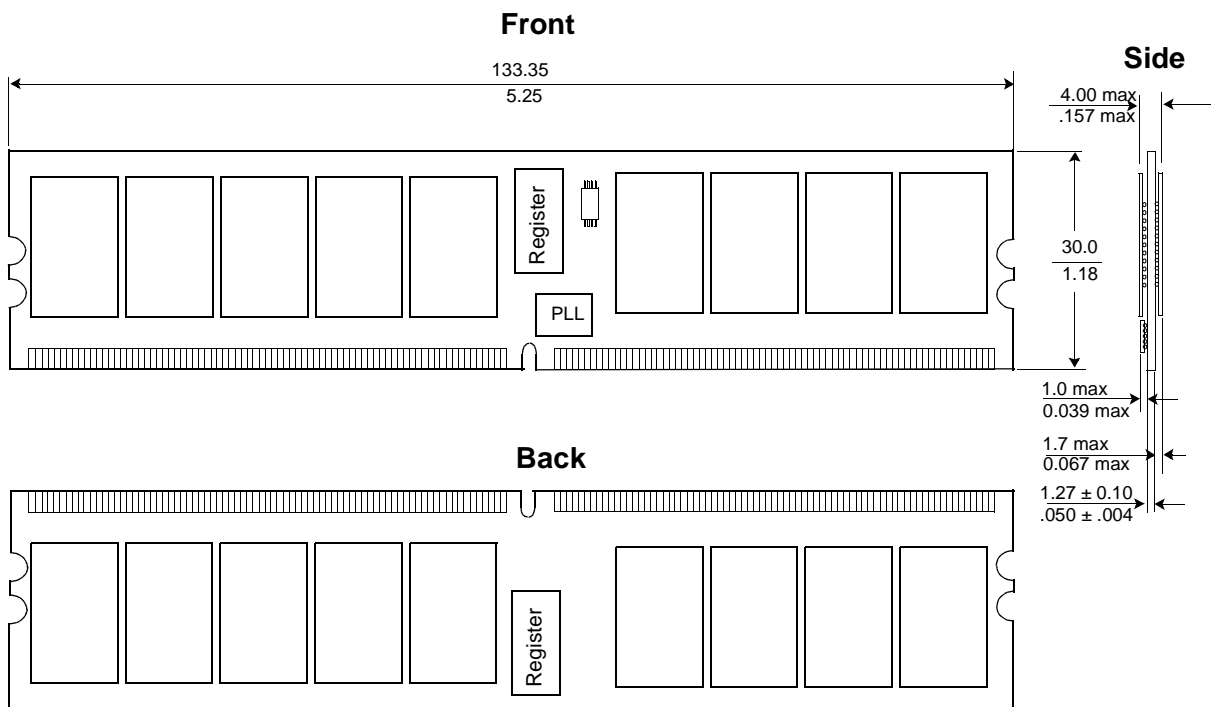
- Notes:
1. MAX storage case temperature T_{STG} is measured in the center of the package, as shown in Figure 11. This case temperature limit is allowed to be exceeded briefly during package reflow, as noted in Micron technical note TN-00-15, "Recommended Soldering Parameters."
 2. MAX operating case temperature T_C is measured in the center of the package, as shown in Figure 11.
 3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
 4. Both temperature specifications must be satisfied.
 5. Operating ambient temperature surrounding the package.

IDD Specifications and Conditions

DC Characteristics 1 (TC = 0 °C to +85 °C, VDD = 1.8 V ±0.1V, VSS = 0V)

Data rate (Mbps)			667		
Parameter	Symbol	max.	Unit	Notes	
Operating one bank active-precharge current: tCK=tCK(IDD),tRC=tRC(IDD),tRAS=tRAS MIN(IDD);CKE is HIGH,S# is HIGH between valid commands;Address bus inputs are switching;Data bus inputs are switching	IDD0	603	mA		
Operating one bank active-read-precharge current: IOUT=0mA;BL=4,CL=CL(IDD),AL=0; tCK=tCK(IDD), tRC=tRC(IDD), tRAS=tRAS MIN(IDD), tRCD=tRCD(IDD);CKE is HIGH between valid commands;Address bus inputs are switching;Data pattern is same as IDD4W	IDD1	693	mA		
Precharge power-down current: All device banks idle; tCK=tCK(IDD);CKE is LOW;Other control and address bus inputs are stable;Data bus inputs are floating	IDD2P	126	mA		
Precharge power-down current: All device banks idle; tCK=tCK(IDD);CKE is HIGH,S# is HIGH;Other control and address bus inputs are stable;Data bus inputs are floating	IDD2Q	432	mA		
Precharge standby current: All device banks idle; tCK=tCK(IDD);CKE is HIGH,S# is HIGH;Other control and address bus inputs are stable;Data bus inputs are floating	IDD2N	432	mA		
Active power-down current: All device banks open; tCK=tCK(IDD);CKE is LOW;Other control and address bus inputs are stable;Data bus inputs are floating	Fast PDN exit MR[12]=0	270	mA		
		Slow PDN exit MR[12]=1			
Active standby current: All device banks open; tCK=tCK(IDD), tRAS=tRAS MAX(IDD), tRP=tRP(IDD); CKE is HIGH,S# is HIGH between valid commands; Other control and address bus inputs are switching;Data bus inputs are switching	IDD3N	540	mA		
Operating burst write current: All device banks open;Continuous burst writes;BL=4,CL=CL(IDD),AL=0; tCK=tCK(IDD), tRAS=tRAS MAX(IDD), tRP=tRP(IDD); CKE is HIGH,S# is HIGH between valid commands;Address bus inputs are switching;Data bus inputs are switching	IDD4W	1098	mA		
Operating burst read current: All device banks open;Continuous burst read, IOUT=0mA;BL=4,CL=CL(IDD),AL=0; tCK=tCK(IDD), tRAS=tRAS MAX(IDD), tRP=tRP(IDD);CKE is HIGH,S# is HIGH between valid commands;Address bus inputs are switching; Data bus inputs are switching	IDD4R	1053	mA		
Burst refresh current: tCK=tCK(IDD);REFRESH command at every tRFC(IDD) interval; CKE is HIGH,S# is HIGH between valid commands; Other control and address bus inputs are switching;Data bus inputs are switching	IDD5	1323	mA		
Self refresh current: CK and CK# at 0V;CKE ≤ 0.2V;Other control and address bus inputs are floating;Data bus inputs are floating	IDD6	126	mA		
Operating bank interleave read current: All device banks interleaving reads, IOUT=0mA;BL=4,CL=CL(IDD),AL=tRCD(IDD)-1x tCK(IDD); tCK=tCK(IDD), tRC=tRC(IDD), tRRD=tRRD(IDD), tRCD=tRCD(IDD); CKE is HIGH,S# is HIGH between valid commands; Address bus inputs are stable during deselects;Data bus inputs are switching	IDD7	1728	mA		

Dimensions



Note: All dimensions are typical unless otherwise stated. $\frac{\text{Millimeters}}{\text{Inches}}$

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them. In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

NOTES FOR CMOS DEVICES

1) PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

2) HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.