DATA SHEET

DDR3 SDRAM
240Pin Registered DIMM
Based on Elpida 2Gb D-die

78-ball FBGA With Lead-Free
(RoHS compliant)

Revision History

Revision No.	History	Draft Date	Remark
1.0	Initial Release	December, 2013	

Features

- Package: 240-pin dual-in-line DDR3 memory module (RDIMM)
- Dansity: 2GB
- Organization: 256Mb*72, 1 Rank
- Power supply: VDD = 1.5 V ±0.075V
- Data rates: 1333Mbps(max.)
  Backward compatible to 1066Mbps
- 8 independent internal banks
- Bi-directional Differential data strobe (DQS, DQS#)
- Differential clock inputs (CK,CK#)
- Commands entered on each rising CK edge
- Eight-bit pre-fetch architecture
- DQS edge-aligned with data for READs
- DQS center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Data mask (DM) for masking write data
- Burst lengths(BL): 8 and 4 with Burst Chop(BC)
- ZQ calibration for DQ drive and ODT
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Operating case temperature range:
  Tc = 0℃ ~ 95℃
- Average refresh period:
  7.8us at 0 ~ 85℃; 3.9us at 85 ~ 95℃
- Asynchronous reset
- Lead-free
- For contact pads, electrolytic gold plating

Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Gold plating thickness(min.)
RMS6061ED58E8W-1333	2GB	256M*72	256Mx8(EDJ2108EDBG-DJ-F) *9	1	0.76um

Detailed Information
For detailed electrical specifications and further information, please refer to the component DDR3L SDRAM datasheet EDJ2108EDBG-DJ-F.

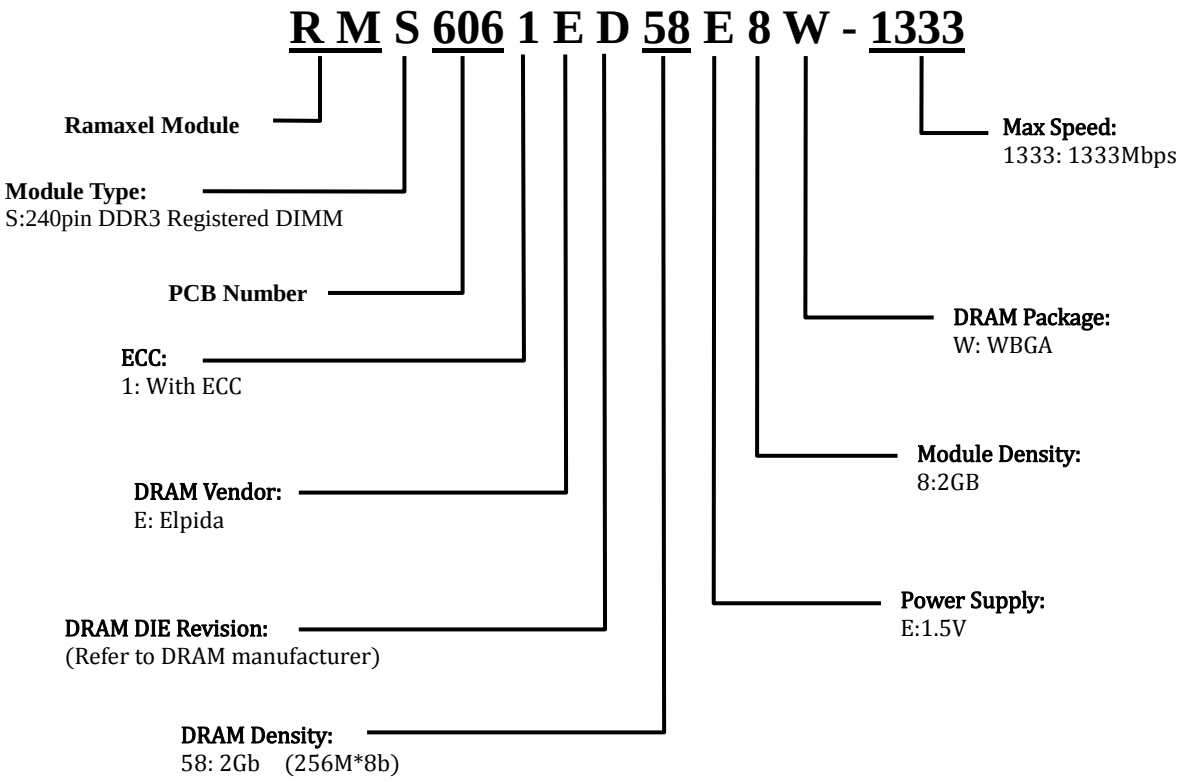
Key Parameters

Speed	DDR3-1066	DDR3-1333	Unit
	7-7-7	9-9-9	
tCK(min)	1.875	1.5	ns
CAS Latency	5,6,7,8	5,6,7,8,9,10	tCK
tRCD(min)	13.125	13.5	ns
tRP(min)	13.125	13.5	ns
tRAS(min)	37.5	36	ns
tRC(min)	50.625	49.5	ns

Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
256*8(2Gb) based module	A0-A14	A0-A9	BA0-BA2	A10/AP

Part Number


R M S 606 1 E D 58 E 8 W - 1333
Ramaxel Module
Module Type:
S:240pin DDR3 Registered DIMM
PCB Number
ECC:
1: With ECC
DRAM Vendor:
E: Elpida
DRAM DIE Revision:
(Refer to DRAM manufacturer)
DRAM Density:
58: 2Gb (256M*8b)
Power Supply:
E:1.5V
Module Density:
8:2GB
DRAM Package:
W: WBGA
Max Speed:
1333: 1333Mbps

Pin Assignments

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREFDQ	121	VSS	31	DQ25	151	VSS	61	A3	181	A1	91	DQ41	211	VSS
2	VSS	122	DQ4	32	VSS	152	DM3/ TDQS12[5]	62	VDD	182	VDD	92	VSS	212	DM5/ TDQS14
3	DQ0	123	DQ5	33	$\overline{DQS}$ 3	153	NC/ $\overline{TDQS}$12[5]	63	CK1/NC[3]	183	VDD	93	$\overline{DQS}$ 5	213	NC/ $\overline{TDQS}$14
4	DQ1	124	VSS	34	DQS3	154	VSS	64	$\overline{CK}$1/NC[3]	184	CK0	94	DQS5	214	VSS
5	VSS	125	DM0/ TDQS9[5]	35	VSS	155	DQ30	65	VDD	185	$\overline{CK}$0	95	VSS	215	DQ46
6	$\overline{DQS}$ 0	126	NC/ $\overline{TDQS}$9[5]	36	DQ26	156	DQ31	66	VDD	186	VDD	96	DQ42	216	DQ47
7	DQS0	127	VSS	37	DQ27	157	VSS	67	VREFCA	187	$\overline{EVENT}$	97	DQ43	217	VSS
8	VSS	128	DQ6	38	VSS	158	NC	68	NC	188	A0	98	VSS	218	DQ52
9	DQ2	129	DQ7	39	NC	159	NC	69	VDD	189	VDD	99	DQ48	219	DQ53
10	DQ3	130	VSS	40	NC	160	VSS	70	A10/AP	190	BA1	100	DQ49	220	VSS
11	VSS	131	DQ12	41	VSS	161	DM8/ TDQS17[5]	71	BA0	191	VDD	101	VSS	221	DM6/ TDQS15[5]
12	DQ8	132	DQ13	42	$\overline{DQS}$ 8	162	NC/ $\overline{TDQS}$17[5]	72	VDD	192	$\overline{RAS}$	102	$\overline{DQS}$ 6	222	NC/ $\overline{TDQS}$15[5]
13	DQ9	133	VSS	43	DQS8	163	VSS	73	$\overline{WE}$	193	$\overline{S}$ 0	103	DQS6	223	VSS
14	VSS	134	DM1/ TDQS10[5]	44	VSS	164	NC	74	$\overline{CAS}$	194	VDD	104	VSS	224	DQ54
15	$\overline{DQS}$ 1	135	NC/ $\overline{TDQS}$10[5]	45	NC	165	NC	75	VDD	195	ODT0	105	DQ50	225	DQ55
16	DQS1	136	VSS	46	NC	166	VSS	76	$\overline{S}$1/NC[2]	196	A13	106	DQ51	226	VSS
17	VSS	137	DQ14	47	VSS	167	NC, TEST[4]	77	ODT1/NC[2]	197	VDD	107	VSS	227	DQ60
18	DQ10	138	DQ15	48	NC	168	$\overline{RESET}$	78	VDD	198	$\overline{S}$ 3	108	DQ56	228	DQ61
19	DQ11	139	VSS	49	NC	169	CKE1/NC[2]	79	NC	199	VSS	109	DQ57	229	VSS
20	VSS	140	DQ20	50	CKE0	170	VDD	80	VSS	200	DQ36	110	VSS	230	DM7/ TDQS16[5]
21	DQ16	141	DQ21	51	VDD	171	A15	81	DQ32	201	DQ37	111	$\overline{DQS}$ 7	231	NC/ $\overline{TDQS}$16[5]
22	DQ17	142	VSS	52	BA2	172	A14	82	DQ33	202	VSS	112	DQS7	232	VSS
23	VSS	143	DM2/ TDQS11[5]	53	NC	173	VDD	83	VSS	203	DM4/ TDQS13[5]	113	VSS	233	DQ62
24	$\overline{DQS}$ 2	144	NC/ $\overline{TDQS}$11[5]	54	VDD	174	A12	84	$\overline{DQS}$ 4	204	NC /$\overline{TDQS}$13[5]	114	DQ58	234	DQ63
25	DQS2	145	VSS	55	A11	175	A9	85	DQS4	205	DQS5	115	DQ59	235	VSS
26	VSS	146	DQ22	56	A7	176	VDD	86	VSS	206	DQ38	116	VSS	236	VDDSPD
27	DQ18	147	DQ23	57	VDD	177	A8	84	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	VSS	58	A5	178	A6	88	DQ35	208	VSS	118	SCL	238	SDA
29	VSS	149	DQ28	59	A4	179	VDD	89	VSS	209	DQ44	119	SA2	239	VSS
30	DQ24	150	DQ29	60	VDD	180	A3	90	DQ40	210	DQ45	120	VTT	240	VTT

Notes

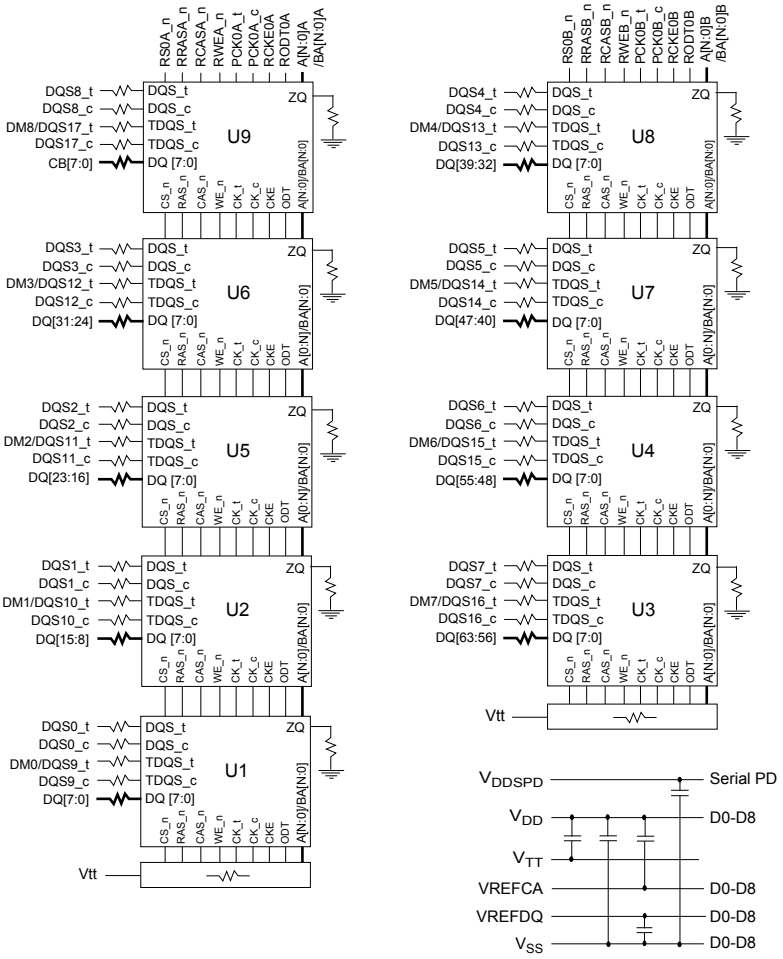
1. NC = No Connect, NU = Not Useable.
2. $\overline{S}$1, ODT1,CKE1: Used for dual-rank DIMMs; NC on single-rank DIMMs
3. CK1,NC and $\overline{CK}$1 ,NC : Used for dual-rank UDIMMs, not used on single-rank DIMMs, but terminated
4. TEST used by memory bus analysis tools (unused on memory DIMMs)
5. DM[0:8] used on UDIMMs,DM8 is not used on x64 UDIMMs;NC,TDQS[9:17] and $\overline{TDQS}$[9:17] used on RDIMMs.

Pin Functional Description

Symbol	Type	Polarity	Function
CK0/$\overline{CK0}$ CK1/$\overline{CK1}$	Input	Cross point	CK and $\overline{CK}$ are differential clock inputs. All the DDR3 SDRAM add/ctrl inputs are sampled on the crossing of positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossing of CK and $\overline{CK}$ (Both directions of crossing).
CKE[0:1]	Input	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S}$[0:1]	Input	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
$\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$	Input	Active Low	$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (along with $\overline{S}$) define the command being entered.
ODT[0:1]	Input	Active High	When high, termination resistance is enabled for all DQ, DQS_t, DQS_c and DM pins, assuming this function is enabled on the DRAM.
DM[0:8]	Input	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
TDQS[9:17], $\overline{TDQS}$[9:17]	Output		TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
DQS[0:8] $\overline{DQS}$[0:8]	I/O	Cross point	Data strobe for input and output data. For raw cards using x16 organized DRAMs, Pins DQ0–DQ7 are asso-ciated with the LDQS and $\overline{LDQS}$ pins and Pins DQ8–DQ15 are associated with UDQS and $\overline{UDQS}$ pins.
BA[0:2]	Input	-	Selects which SDRAM bank of eight is activated.
A0- A15	Input	-	During a Bank Activate command cycle, Address input defines the row address (RA0–RA15).During a Read or Write command cycle, Address input defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, auto-precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12($\overline{BC}$) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped).
DQ[0:63] CB0-CB7	I/O	-	Data and Check Bit Input/Output pins.
VDD, VSS	Supply	-	Power and ground for the DDR3 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to VDD/VDDQ planes on these modules.
VDDQ	Supply	-	Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins.
VDDSPD	Supply	-	Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 3.0V to 3.6V
VREFDQ	Supply	-	Reference voltage for I/O inputs.
VREFCA	Supply	-	Reference voltage for command/address inputs.
SDA	I/O	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to VDDSPD to act as a pullup on the system board
SCL	Input	-	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to VDDSPD to act as a pullup on the system board.
SA[0:2]	Input	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.
$\overline{EVENT}$	Output	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the $\overline{EVENT}$ pin on the TS/SPD part
$\overline{RESET}$	Input	Active Low	The $\overline{RESET}$ pin is connected to the $\overline{RESET}$ pin on each DRAM. When low, all DRAMs are set to a known state.

Block Diagram

Raw Card K0 (x72 DIMM, populated as one physical ranks of x8 DDR3 SDRAMs)



NOTE 1 DQ-to-I/O wiring may be changed within a byte.
NOTE 2 ZQ resistors are 240 Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.
NOTE 3 The connection of the Serial PD to EVENT_n (Option 1) or to ground (Option 2) is realized by resistor options.

Electrical Specifications

All voltages are referenced to VSS (GND).

Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to VSS	-0.4 ~ 1.975	V	1
VDDQ	Voltage on VDDQ pin relative to VSS	-0.4 ~ 1.975	V	1
VIN, VOUT	Voltage on any pin relative to VSS	-0.4 ~ 1.975	V	1
TSTG	Storage Temperature	-55 ~ +100	℃	1,2

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

Module Temperature Condition

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	Tc	0 to +95	℃	1,2,3

Notes:

1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85℃ under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85℃ and 95℃ case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9μs. (This double refresh requirement may not apply for some devices.)

b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

DC/AC Operating Condition

Recommended DC Operating Conditions - DDR3 (1.5V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2,3
VDDQ	Supply Voltage for OutpuT	1.425	1.5	1.575	V	1,2,3
VrefCA(DC)	Input reference voltage for address, command inputs	0.49*VDD	-	0.51*VDD	V	4,5,
VrefDQ(DC)	Input reference voltage for DQ, DM inputs	0.49*VDD	-	0.51*VDD	V	4,5,

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. The AC peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than ±1% VDD (for reference: approx ±15 mV).
4. For reference: approx. VDD/2 ±15 mV.

IDD Specifications and Conditions

• DC Characteristics 1 (TC = 0 ℃ to +85 ℃, VDD = 1.5 V ±0.075V, VSS = 0V)

Data rate (Mbps)		1333	1066		
Parameter	Symbol	max.	max.	Unit	Notes
Operating current (ACT-PRE)	IDD0	450	405	mA	
Operating current (ACT-READ-PRE)	IDD1	540	495	mA	
Precharge power-down standby	IDD2P0	108	108	mA	Slow PD Exit
	IDD2P1	162	162	mA	Fast PD Exit
Precharge standby current	IDD2N	270	243	mA	
Precharge standby ODT current	IDD2NT	270	243	mA	
Precharge quiet standby current	IDD2Q	270	243	mA	
Active power-down current(Always fast exit)	IDD3P	243	243	mA	
Active standby current	IDD3N	360	333	mA	
Operating current (Burst read operating)	IDD4R	900	810	mA	
Operating current (Burst write operating)	IDD4W	945	855	mA	
Burst refresh current	IDD5B	1530	1530	mA	
All bank interleave read current	IDD7	1530	1350	mA	
RESET low current	IDD8	108	108	mA	

• Self-Refresh Current (TC = 0 ℃ to +85 ℃, V VDD = 1.5 V ±0.075V)

Parameter	Symbol	max.	Unit	Notes
Self-refresh current normal temperature range	IDD6	108	mA	
Self-refresh current extended temperature range	IDD6ET	162	mA	
Auto self-refresh current (optional)	IDD6TC	-	mA	

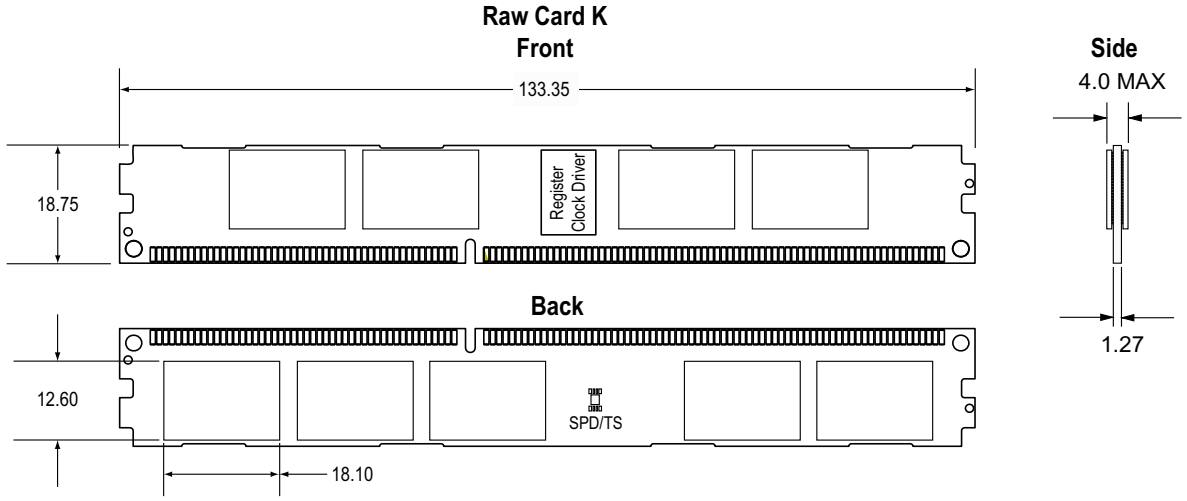
SPD Matrix

Byte No.	Function described	Function support	Hex
0	Number of Serial PD Bytes Written/ SPD Device Size / CRC Coverage	176/256/0-116	92
1	SPD Revision	Version 1.1	11
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	RDIMM	01
4	SDRAM Density and Banks	8 banks,2Gb	03
5	SDRAM Addressing	15 Row×10 Col	19
6	Module Nominal Voltage, VDD	1.5V	00
7	Module Organization	1Ranks x8	01
8	Module Memory Bus Width	72bits/ECC	0B
9	Fine Timebase (FTB) Dividend/Divisor	2.5ps	52
10	Medium Timebase (MTB) Dividend	0.125ns	01
11	Medium Timebase (MTB) Divisor		08
12	SDRAM Minimum Cycle Time (tCKmin)	DDR3 1333	0C
13	Reserved	Reserved	00
14	CAS Latencies Supported, LSB	10,9,8,7,6,5,	7E
15	CAS Latencies Supported, MSB	-	00
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6ns	30
20	Minimum Row Precharge Delay Time (tRPmin)	13.125ns	69
21	Upper Nibbles for tRAS and tRC	Refer to Byte22,23	11
22	Minimum Active to Precharge Delay Time (tRASmin), LSB	36ns	20
23	Minimum Active to Active/Refresh Delay Time (tRCmin), LSB	49.125ns	89
24	Minimum Refresh Recovery Delay Time (tRFCmin), LSB	160ns	00
25	Minimum Refresh Recovery Delay Time (tRFCmin), MSB		05
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	30ns	00
29	Minimum Four Activate Window Delay Time (tFAWmin)	30ns	F0
30	SDRAM Optional Features	Dll-off,RZQ/7,6	83
31	SDRAM Thermal and Refresh Options	PASR,2X at 85-95℃, 0-95℃	81
32	Module Thermal Sensor	incorporated	80
33	SDRAM Device Type	Standard	00
34-59	Reserved	Reserved	00
60	Module Nominal Height	18.75mm	04
61	Module Maximun Thickness	F:1-2mm, B:1-2mm	11
62	Reference Raw Card Used	Raw Card: L0	09
63	DIMM Module Attributes	1 row,1 register	05
64	RDIMM Thermal Heat Spreader Solution		00
65	Register Manufacturer ID Code, LSB		86

66	Register Manufacturer ID Code, MSB		32
67	Register Revision Number		10
68	Register Type		00
69	RC1 (MS Nibble) / RC0 (LS Nibble)		C0
70	RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength,Command/Address		00
71	RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength,Control and Clock		00
72	RC7 (MS Nibble) / RC6 (LS Nibble) - Reserved for Register Vendor Specific Modes		00
73	RC9 (MS Nibble) / RC8 (LS Nibble) - Reserved		00
74	RC11 (MS Nibble) / RC10 (LS Nibble) - Reserved		00
75	RC13 (MS Nibble) / RC12 (LS Nibble) - Reserved		00
76	RC15 (MS Nibble) / RC14 (LS Nibble) - Reserved		00
77-116	Reserved		00
117	Module ID: Module Manufacturer's JEDEC ID Code	Ramaxel	04
118	Module ID: Module Manufacturer's JEDEC ID Code		43
119	Module ID: Module Manufacturing Location	Shenzhen	01
120-121	Module ID: Module Manufacturing Date		00
122-125	Module ID: Module Serial Number		00
126	Cyclical Redundancy Code(CRC)		38
127	Cyclical Redundancy Code(CRC)		7E
128-145	Module Part Number	R	52
129		M	4D
130		S	53
131		6	36
132		0	30
133		6	36
134		1	31
135		E	45
136		D	44
137		5	35
138		8	38
139		E	45
140		8	38
141		W	57
142		1	31
143		3	33
144		3	33
145		3	33
146	Module Revision Code	A	41
147	Module Revision Code		00
148	DRAM Manufacturer's JEDEC ID Code, LSB	Elpida	02
149	DRAM Manufacturer's JEDEC ID Code, MSB	Elpida	FE
150-175	Manufacturer's Specific Data		00
176-255	Open for customer use		00

Dimensions

Unit: mm



*Note: Tolerances on all dimensions ±0.15 unless otherwise specified.

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stresson these components to prevent damaging them.In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

NOTES FOR CMOS DEVICES

1) PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

2) HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.